METHOD OF FORMING A SEMICONDUCTOR STRUCTURE COMPRISING AN IMPLANTATION OF IONS IN A MATERIAL LAYER TO BE ETCHED

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present disclosure generally relates to the fabrication of integrated circuits, and, more specifically, to methods of forming a semiconductor structure wherein ions are implanted into a material layer to modify an etch rate of the material layer in an etching process.

[0003] 2. Description of the Related Art

[0004] Integrated circuits comprise a large number of individual circuit elements, e.g., transistors, capacitors and resistors. These elements are connected internally to form complex circuits such as memory devices, logic devices and microprocessors. The performance of integrated circuits may be improved by increasing the number of functional elements per circuit in order to increase their functionality and/or by increasing the speed of operation of the circuit elements. A reduction of feature sizes allows the formation of a greater number of circuit elements on the same area, hence allowing an extension of the functionality of the circuit, and also reduces signal propagation delays, thus making an increase of the speed of operation of circuit elements possible.

[0005] Field effect transistors are used as switching elements in integrated circuits. They provide a means to control a current flowing through a channel region located between a source region and a drain region. The source region and the drain region are highly doped. In N-type transistors, the source and drain regions are doped with an N-type dopant. Conversely, in P-type transistors, the source and drain regions are doped with a P-type dopant. The doping of the channel region is inverse to the doping of the source region and the drain region. The conductivity of the channel region is controlled by a gate voltage applied to a gate electrode formed above the channel region and separated therefrom by a thin insulating layer. Depending on the gate voltage, the channel region may be switched between a conductive "on" state and a substantially non-conductive "off" state.

[0006] When reducing the size of field effect transistors, it is important to maintain a high conductivity of the channel region in the "on" state. The conductivity of the channel region in the "on" state depends on the dopant concentration in the channel region, the mobility of the charge carriers, the extension of the channel region in the width direction of the transistor and on the distance between the source region and the drain region, which is commonly denoted as "channel length." While a reduction of the width of the channel region leads to a decrease of the channel conductivity, a reduction of the channel length enhances the channel conductivity. An increase of the charge carrier mobility leads to an increase of the channel conductivity.

[0007] As feature sizes are reduced, the extension of the channel region in the width direction is also reduced. A reduction of the channel length entails a plurality of issues associated therewith. First, advanced techniques of photolithography and etching have to be provided in order to reliably and reproducibly create transistors having short channel lengths. Moreover, highly sophisticated dopant profiles, in the vertical direction as well as in the lateral direction, are required in the source region and in the drain region in order to provide a low sheet resistivity and a low contact resistivity in combination with a desired channel controllability.

[0008] In view of the problems associated with a further reduction of the channel length, it has been proposed to also enhance the performance of field effect transistors by increasing the charge carrier mobility in the channel region. In principle, at least two approaches may be used to increase the charge carrier mobility.

[0009] First, the dopant concentration in the channel region may be reduced. Thus, the probability of scattering events of charge carriers in the channel region is reduced, which leads to an increase of the conductivity of the channel region. Reducing the dopant concentration in the channel region, however, significantly affects the threshold voltage of the transistor device. This makes the reduction of dopant concentration a less attractive approach.

[0010] Second, the lattice structure in the channel region may be modified by creating tensile or compressive stress. This leads to a modified mobility of electrons and holes, respectively. Depending on the magnitude of the stress, a compressive stress may significantly increase the mobility of holes in a silicon layer. The mobility of electrons may be increased by providing a silicon layer having a tensile stress.

[0011] A method of forming a semiconductor structure comprising field effect transistors wherein the channel region is formed in stressed silicon will be described in the following with reference to FIGS. **1***a*-**1***d*.

[0012] FIG. **1***a* shows a schematic cross-sectional view of a semiconductor structure **100** in a first stage of a manufacturing process according to the state of the art. The semiconductor structure **100** comprises a substrate **101**. In the substrate **101**, a first active region **104** and a second active region **204** are provided. A trench isolation structure **102** electrically insulates the active regions **104**, **204** from each other and from other elements of the semiconductor structure **100** which are not shown in FIG. **1***a*.

[0013] A gate electrode **106** which is separated from the substrate **101** by a gate insulation layer **105** is formed over the first active region **104**. The gate electrode **106** is covered by a cap layer **107** and flanked by a sidewall spacer structure **108**. The active region **104**, the trench isolation structure **102**, the gate electrode **106**, the gate insulation layer **105**, as well as the first sidewall spacers **108**, **109** and the cap layer **107** together form portions of a first field effect transistor element **130**.

[0014] The semiconductor structure **100** further comprises a second transistor element **230**. Similar to the first transistor element **130**, the second transistor element **230** comprises a gate electrode **206**, a gate insulation layer **205** and a sidewall spacer structure **208**. A cap layer **207** covers the gate electrode **206**.

[0015] In the formation of the semiconductor structure **100**, the substrate **101** is provided and the trench isolation structure **102** is formed by means of methods of photolithography, deposition and/or oxidation known to persons skilled in the art. Then, ions of a dopant material are implanted into the substrate **101** in order to form the active regions **104**, **204**. The type of dopant corresponds to the doping of the channel regions of the transistor elements **130**, **230** to be formed. Hence, if the first transistor element **130** and the second transistor element **230** are N-type transistors, ions of a P-type dopant are implanted, and ions of an N-type dopant may be implanted if the first transistor element **130** and the second transistor element **230** are P-type transistors. In other examples of manufacturing methods according to the state of